IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate including first and second element-formation regions which are partitioned by an isolation trench;

first and second lower gate insulating films formed on the first and second element-formation regions, respectively;

first and second floating gates formed on the first and second lower gate insulating films, respectively, the first floating gate including a first side surface and the second floating gate including a second side surface which is opposed to the first side surface, each of the first and second floating gates including an upper surface;

an isolation insulating film which is formed at least in the isolation trench and which [[has]] includes a depression formed in an upper surface thereof and an uppermost portion located higher than a surface of the semiconductor substrate and lower than the upper surface of each of the first and second floating gates;

an upper gate insulating film formed on the first and second floating gates and the isolation insulating film; and

a control gate line formed on the upper gate insulating film, and including an opposed portion which is opposed to the first and second floating gates, ~~with the upper gate insulating film being interposed,~~ and a portion located inside the depression so that each of the first and second side surfaces of the first and second floating gates is entirely opposed to the control gate line,

the first side surface of the first floating gate entirely aligning with ~~the first floating gate including~~ a side surface included in the first element-formation region and defined by the isolation trench, and the second side surface of the second floating gate ~~including a side surface which is opposed to the first floating gate and which entirely aligns~~ entirely aligning

with a side surface included in the second element-formation region and defined by the isolation trench.

2. (Canceled).

3. (Canceled).

4. (Currently Amended) The semiconductor device according to claim [[3]] 1, wherein the opposed portion of the control gate line is opposed to the upper surfaces of the first and second floating gates and is opposed to those portions of the first and second side surfaces of the first and second floating gates which are located higher than the uppermost portion of the isolation insulating film.

5. (Canceled).

6. (Currently Amended) The semiconductor device according to claim 1, wherein the control gate line includes a lowermost portion located lower than the surface of the semiconductor substrate.

7. (Canceled).

8. (Canceled).

9. (Original) The semiconductor device according to claim 1, wherein the isolation insulating film has a thickness smaller than a half of a width of the isolation trench.

10. (Original) The semiconductor device according to claim 1, wherein the isolation insulating film is formed by CVD.

11. (Withdrawn) A method of manufacturing a semiconductor device comprising:

forming a lower gate insulating film on a semiconductor substrate;

forming a floating gate material film on the lower gate insulating film;

patterning the floating gate material film, the lower gate insulating film and the semiconductor substrate to form first and second pattern regions partitioned by a trench;

forming a lower insulating film having a first depression in the trench;

forming an upper insulating film on the lower insulating film to fill the first depression with the upper insulating film;

etching the upper insulating film at an etching rate higher than an etching rate of the lower insulating film to form a second depression corresponding to the first depression in the lower insulating film;

forming an upper gate insulating film on the patterned floating gate material films included in the first and second pattern regions; and

forming a control gate material film on the upper gate insulating film and in the second depression.

12. (Withdrawn) The method according to claim 11, further comprising patterning the control gate material film, the upper gate insulating film and the patterned floating gate material films by use of a mask pattern substantially perpendicular to the trench.

13. (Withdrawn) The method according to claim 11, wherein the lower insulating film having the second depression includes an uppermost portion located higher than lower surfaces of the patterned floating gate material films included in the first and second pattern regions.

14. (Withdrawn) The method according to claim 11, wherein etching the upper insulating film includes etching an upper portion of the lower insulating film, and the lower

insulating film after being etched includes an uppermost portion located lower than upper surfaces of the patterned floating gate material films included in the first and second pattern regions.

15. (Withdrawn) The method according to claim 11, wherein the control gate material film formed in the second depression includes a lowermost portion located lower than lower surfaces of the patterned floating gate material films included in the first and second pattern regions.

16. (Withdrawn) The method according to claim 11, wherein forming the lower insulating film in the trench includes forming the lower insulating film outside the trench, and wherein the method further comprises removing the upper and lower insulating films formed outside the trench before etching the upper insulating film.

17. (Withdrawn) The method according to claim 11, wherein forming the control gate material film in the second depression includes filling the second depression with the control gate material film.

18. (Withdrawn) The method according to claim 11, wherein the lower insulating film having the first depression has a thickness which is smaller than a half of a width of the trench.

19. (Withdrawn) The method according to claim 11, wherein the lower insulating film is formed by CVD, and the upper insulating film is formed by coating.

20. (Withdrawn) The method according to claim 19, wherein the lower insulating film is made of silicon oxide, and the upper insulating film is made of polysilazane first element-

formation region and defined by the isolation trench, and the second floating gate including a side surface which is opposed.

21. (New) The semiconductor device according to claim 1, wherein the depression includes a tapered U-shaped bottom portion.